Flip Chip Tutorial

Presenters/Hosts Sultan Lilani, Richard McKee, Matt Bergeron, & Jeff Schaefer

(sultan.Lilani@integra-tech.com, richard.mckee@integra-tech.com, matt.Bergeron@integra-tech.com, jeff.Schaefer@integra-tech.com)

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Agenda/Topics Covered

1 Session 1 - Overview

a) Flip Chip Definition
b) Benefits
c) Industries Where Used
d) Bumping and RDL
e) Substrate
f) Implementations

2 Session 2 – Assembly & Process

a) Assembly Considerations
b) Process Considerations
c) Process Steps

3 Session 3 – Test and Qualification

Overview

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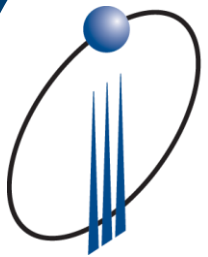

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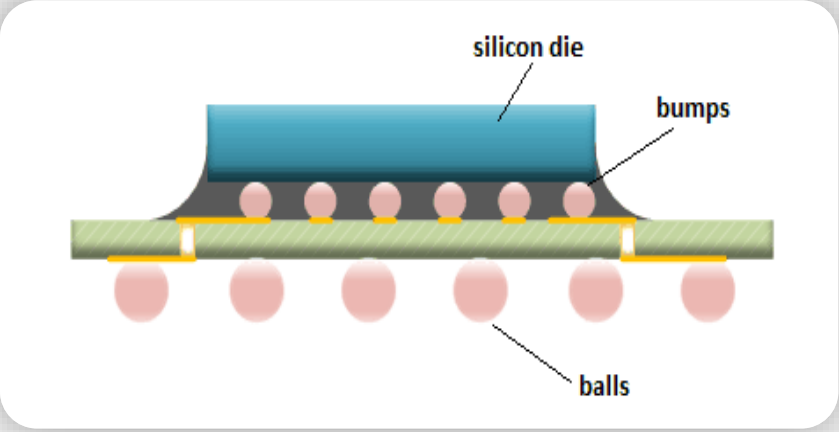
Flip Chip Definition

- Essentially, the name “Flip Chip” describes the method used to connect a semiconductor die to a substrate: The dies are bumped and then “flipped” onto a substrate, hence the name “Flip Chip”.



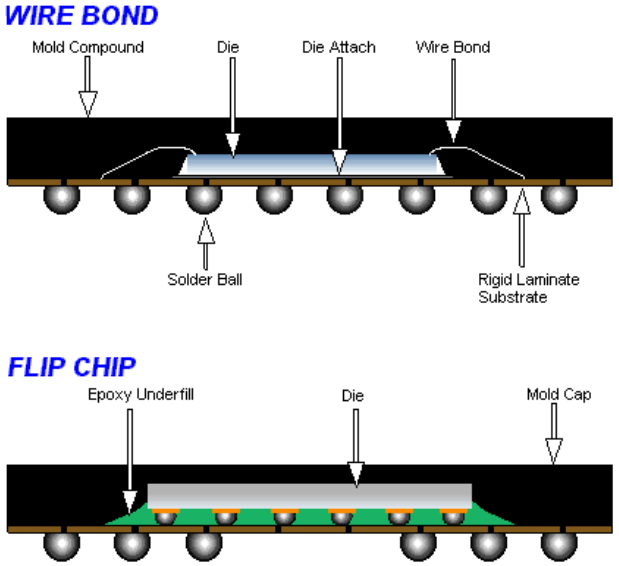
Fundamentals

- Bumps are placed directly on the die I/O pads typically distributed in an array across the entire die surface. This allows designers to place more pads per die, reduce the die size, and optimize signal integrity,
- Following the bumping process, the wafer may be thinned (back grinding), and then diced into individual die separated from the wafer.
- The bumped die is “flipped” onto the substrate. The bumps connect the die and the substrate together into a single package.

Flip Chip: Benefits

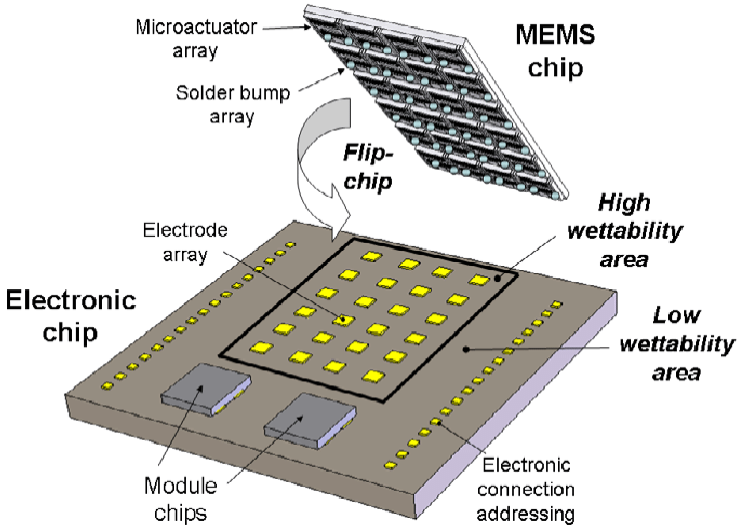
Flip Chip package technology offer a range of benefits including:

- High pin count
- High signal density
- Better power dissipation
- Low signal inductance, and good power/ground connectivity.
- Ideal for high speed interfaces (including RF) that wire bonds cannot support
- Good Assembly dynamics



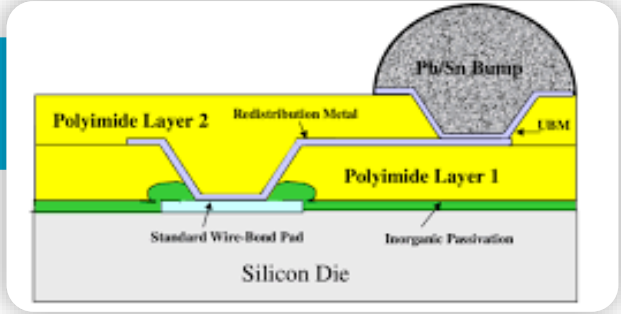
Industries/Applications

- **Traditional**
  - Wireless and Communications
    - Shorter path from die to substrate
  - Space consideration applications
    - Handheld/bodyworn, etc
- **Today's Applications**
  - Automotive
  - Military/Aerospace
  - Computing
  - Life Sciences



Flip Chip: Bump on Pad & RDL

Wafer Bumping can be considered as a step in wafer processing where solder spheres are attached to the I/O pads.



Wafer Bumping Technology

- Some wafers are designed to be flip chips and bumps go directly on pads.
- A Redistribution layer (RDL) is added to a wirebond die to establish bumps that are compatible with the assembly of a die on a Printed Circuit board
- Paste-printed bumps, plated bumps, or placed preformed solder spheres are typically mounted onto a fluxed, under bump metallization (UBM) material, that is plated or sputtered onto the die pads (Al or Cu), to insure good adhesion of the bumps.
- Wafer bump compositions: gold, eutectic, lead tin, lead free, high lead materials, or Cu pillar. The bump size and bump pitch may vary depending on pad count, signal integrity, and assembly design rules.

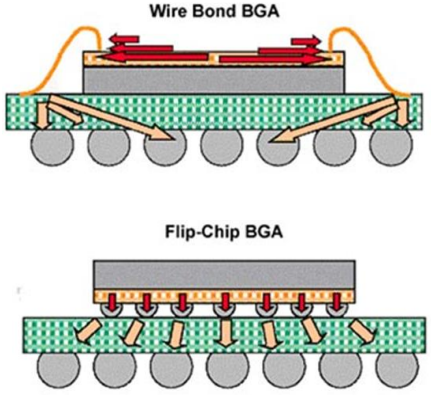
Flip Chip: Substrate Overview

Substrate Technology

- Substrates can be made by different PCB materials: laminate, build-up, organic, ceramic, and more. Substrate layout design rules vary from different suppliers.
- The substrate provides the connectivity to the external PCB via solder balls (typically larger than the bumps, on a broader pad pitch).
- The substrate size, number of layers and material properties have direct impact on the total package cost. In some cases the substrate can be the most expensive element in a Flip Chip package.
- Substrate design consists of layout of all signals from the package external balls to the bumped internal pads.
- Substrates can consist of many layers ranging from 2-18 layers to allow proper routing of all signals for enhanced device performance

Flip Chip Size Considerations

- Is there enough room to actually route the connections from the bumps to the solder balls that connect to the PCB?
- The smaller the substrate vs. the die, the higher the cost in many cases



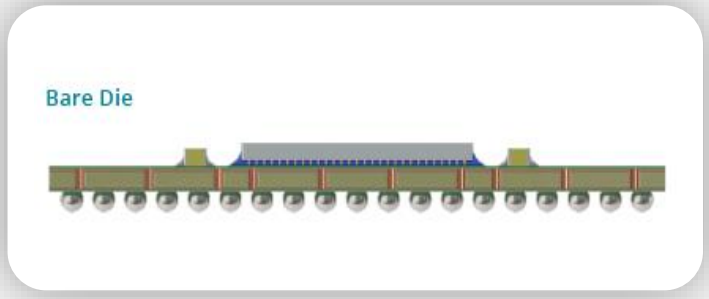
Flip Chip: FCBGA - Package Example

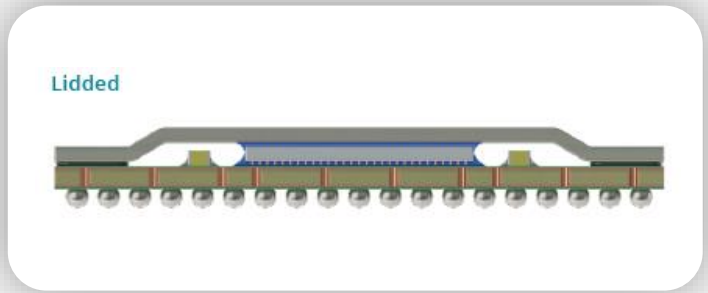
FCBGA – Flip Chip Ball Grid Array

- Flip Chip BGA packages: Still the most common package for bumped dies.

- Advantages:
- Good thermal performance, and scalability for large and complex dies.
- Low cost FCBGAs use a laminate (PCB type) substrate.
- Build-up substrates are also an option, offering –
- Finer pitch routing, enhanced signal and thermal performance, and a lower profile, at a cost.

- FCBGA is the preferred flip chip solution for high power designs and designs with a large number of balls (over 100, for example).



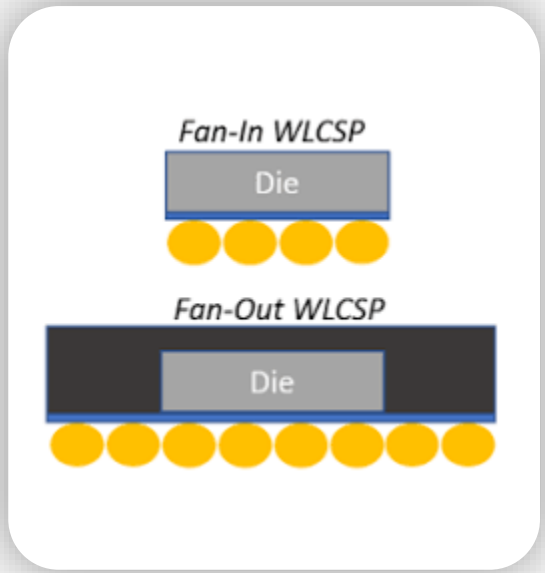


Flip Chip: WLCSP - Package Example

WLCSP – Wafer Level Chip Scale Package – NO Substrate

- **FAN-IN**
  - Wafer Level Chip Scale Package (WLCSP) is a die-sized package with bumps that are essentially balls that can be soldered directly to a PCB.
  - Bump on Pad (BOP): Solder bumps attached directly to the die pad openings, that gives the shortest path from die circuit to PCB, so achieves optimum signal performance, lowest inductance, highest speed).
  - Preferred solution for low-power, low ball count devices where the small form factor is an advantage.

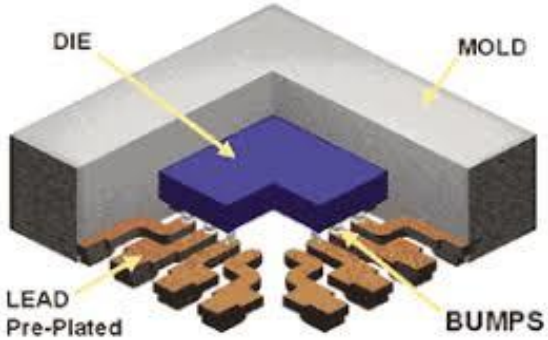
- **FAN-OUT**
  - eWLB is similar to the WLCSP, however the wafers are first diced, the dies spaced apart on tape & frame, and a resin material is flowed over the dies then hardened to form a re-constituted wafer.
  - Referred to as “Fan Out” because the relatively small pitch die pads are able to be routed out (fanned out) to a larger pitch array of balls over the peripheral epoxy resin.



Flip Chip: QFN - Package Example

FCQFN – Flip Chip Quad Flat No Lead

- Flip Chip QFN packages: Copper Leadframe with overmold replaces use of laminate substrate in this popular package for bumped dies. Advantages -
- Self-inductance & capacitance: 60% improvement.
- 15% lower thermal resistance.
- 30x reduction in resistance vs wire bond.
- Withstands 260°C solder shock test.
- Finer pitch routing, enhanced signal and
- thermal performance, with a lower profile.
- FCQFN is the preferred flip chip solution for:
- Wireless Devices.
- Power Management Devices.
- High-speed Network Devices.



Assembly and Process

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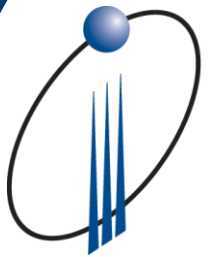

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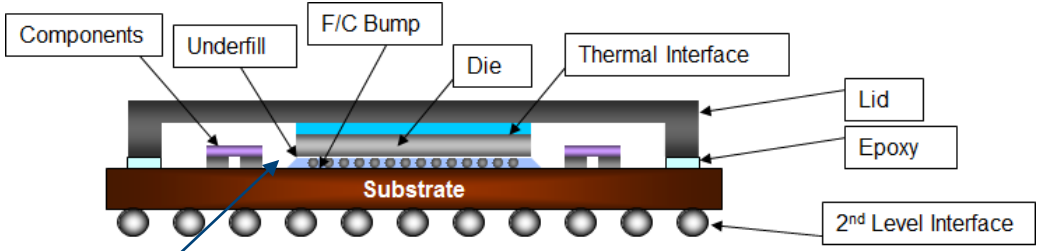
Flip Chip: Design and Assembly Considerations

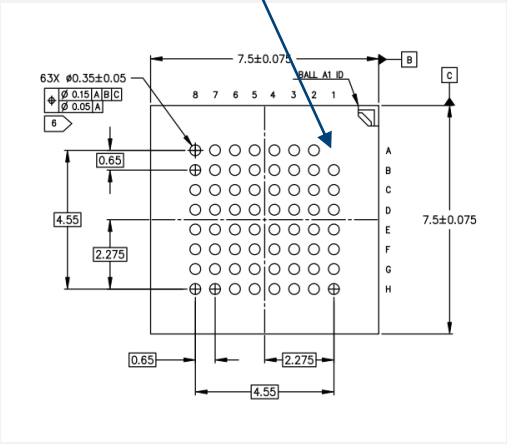


Components should be at least 0.5mm away from FC die for underfill purposes

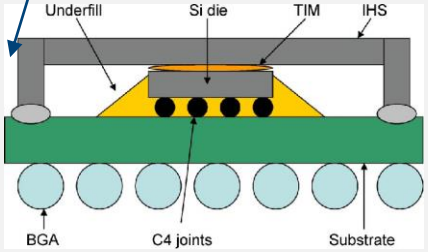
Description	Options	Details / Experience
Substrate	Ceramic, Organic laminate, Flex Circuit, PCB	
Die	Si / SiGe / GaAs / Low K	I/O = 3 min to ~ X (bumps)
Lid / Heat Spreader	Ceramic /Aluminum / Cu	
	Lid Stiffner / No lid	
Thermal Interface	Grease / Gel / Adhesive	
Underfill	Namics 8439-1 / Other(s)	
SMT Components	Resistors, Capacitors, etc. *(high quantities are subject to review)*	Conductive epoxy / Solder
F/C Bump	Eutectic PbSn: 37/63	Pitch = 125um min
	SAC or other Pb-free	Pitch = 125um min
	High Pb: 90/10, 95/5, 97/3	Pitch = 125um min
2nd Level Interface	LGA	Pitch = 0.4 mm min
	BGA [Eutectic / Pb-free]	Pitch = 0.4 mm min
Substrate Metalization	Ceramic	Ni/Au
	Organic	Solder on Pad (SOP) / ENiG

Flip Chip: Design and Assembly Considerations

- **Having an Unique bump pattern will help ensure correct orientation**
  - Note Missing bump below as example



- **Rules for the Lid and Marking**
  - Lid size should be roughly 2mm smaller than substrate
  - Lid should have weeping holes on corners
  - Lid marking should be considered and be executed with a laser.

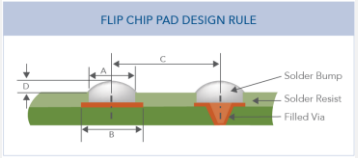


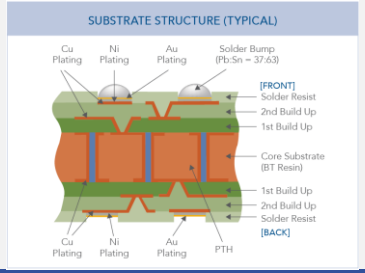
Design Considerations

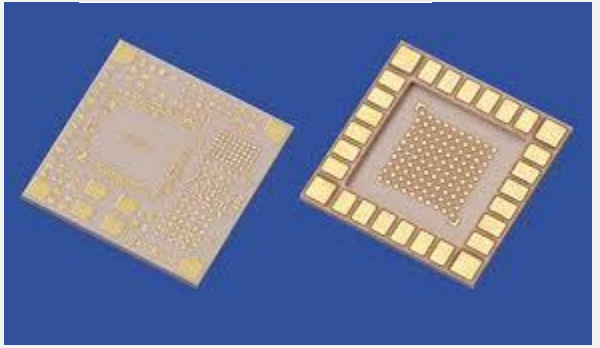
– **Substrate materials**
  - Laminate
  - Ceramic

– **Plating Structure**
  - NiAu for Solderbumps
  - SOP (solder on pad) for Cu Pillar
  - No OSP for BGA Solderballs

– **Non-Standard Materials**
  - Consider minimum order quantities and expiration dates when specifying materials

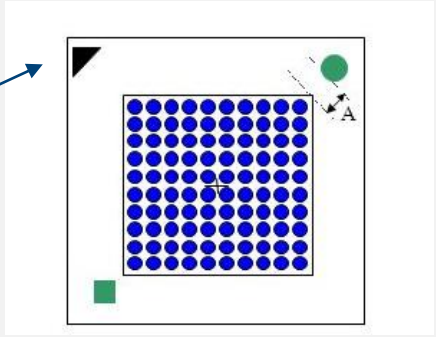




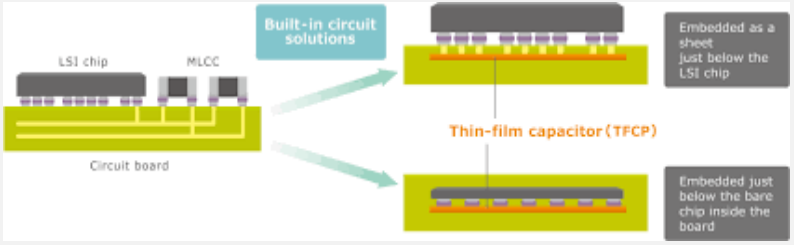


Design considerations

- **Fiducials**
  - Critical in design stage to ease assembly
  - Use an easy to recognize shape for orientation (or multiple marks)

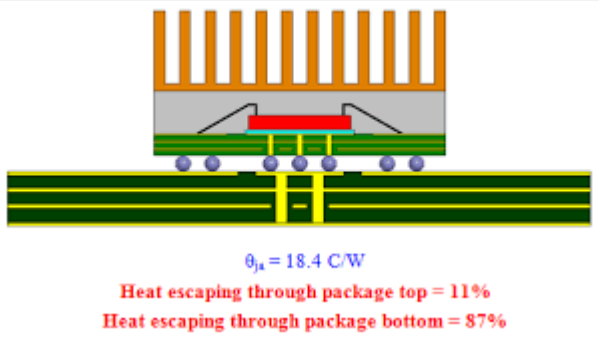


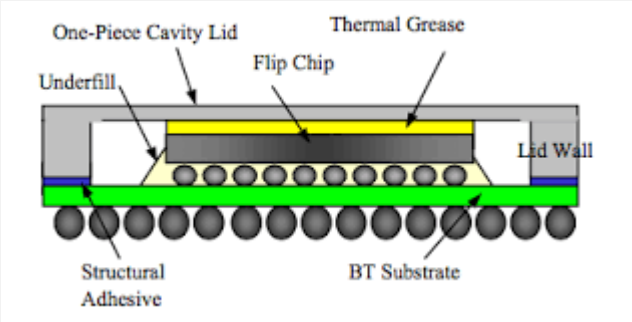
- **Chip caps**
  - Must there be decoupling Capacitors on the package?
  - Can the Capacitors be on the system board?



Design Considerations

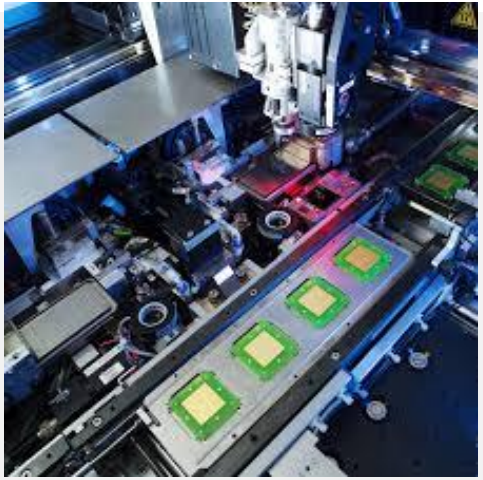
- **Encapsulation**
  - Is plastic necessary/desired
  - Is heat a consideration
- **Heat dissipation**
  - Consider lid/heatsink and substrate heat dissipation
  - Thermal conductivity requirements and Material set match-ups
    - CTEs of die, substrate, PCB, etc.

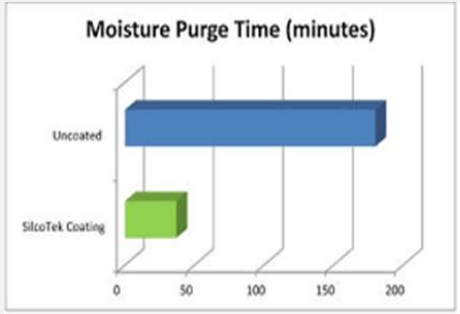




Assembly Considerations

- Assembly considerations
  - Vision system contrast
  - Plasma Clean
  - Acetone use
  - Other component placements
  - Preheating parts for moisture removal
  - Other process Steps (where to put Flip chip)





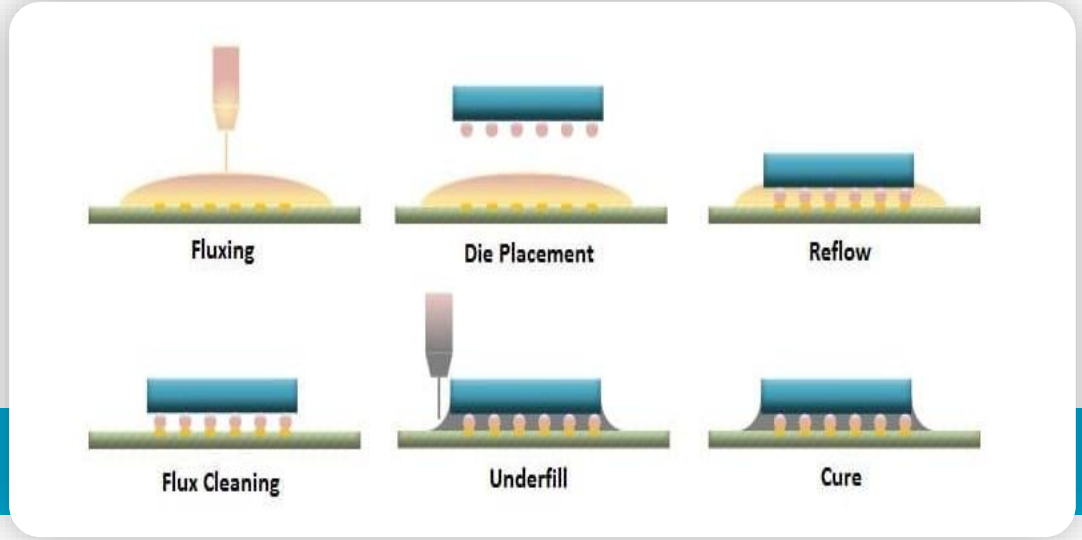
Flip Chip: Assembly Process (FCBGA)

Flip Chip Assembly Process

In order for the chip to be connected or mounted to a substrate, the die is turned or flipped over and brought into alignment with the pads located on the substrate.

There are six (6) key process steps:

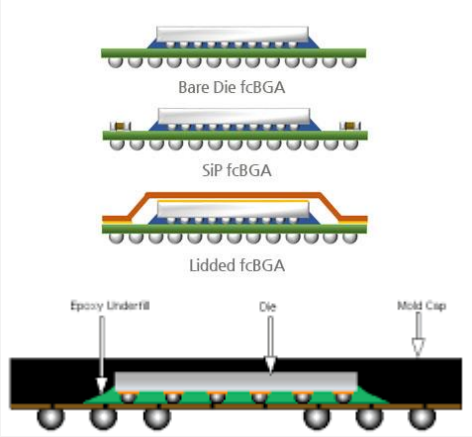
1. **Fluxing**
2. **Placement**
3. **Reflow**
4. **Flux Cleaning**
5. **Capillary Underfill**
6. **Cure**

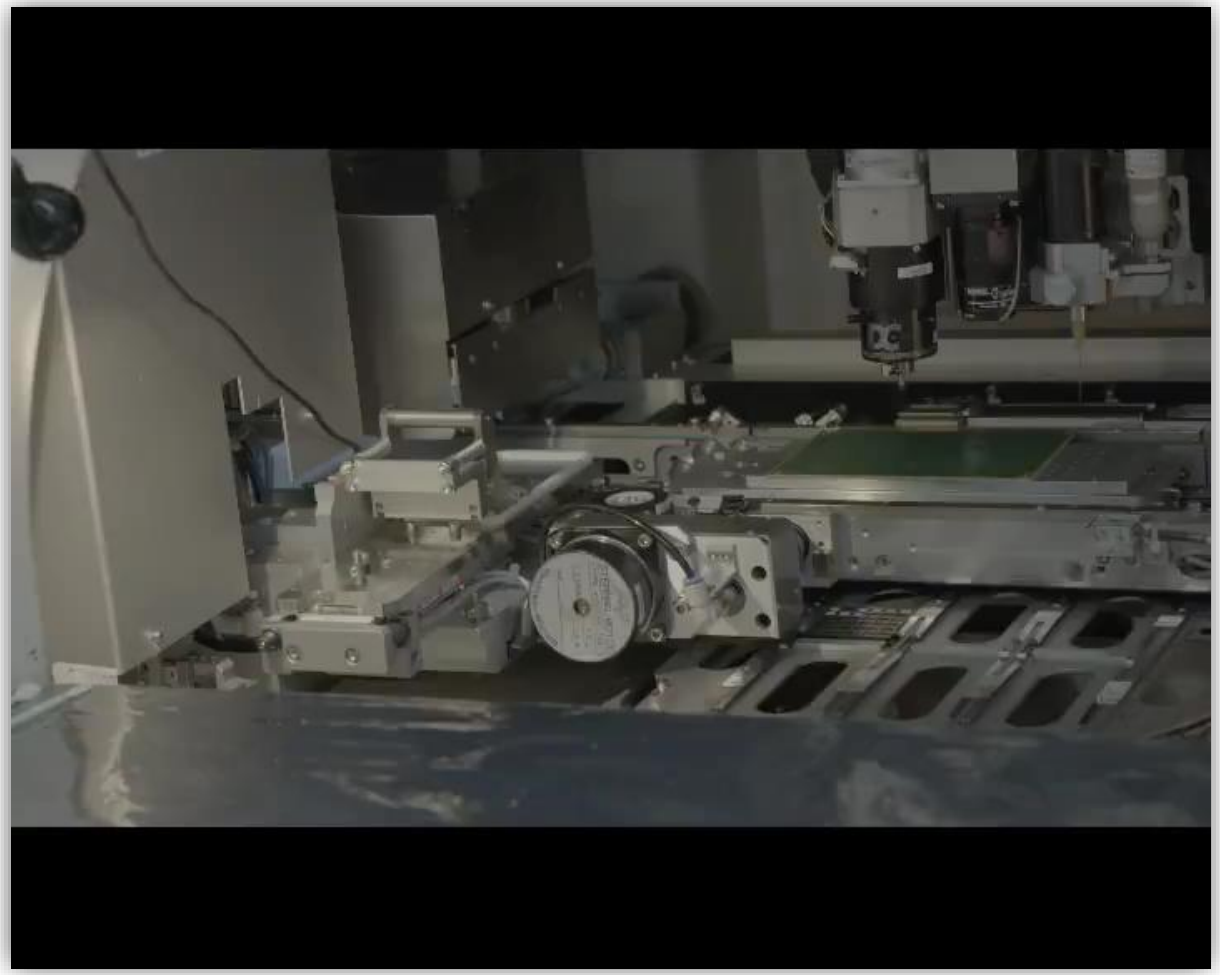


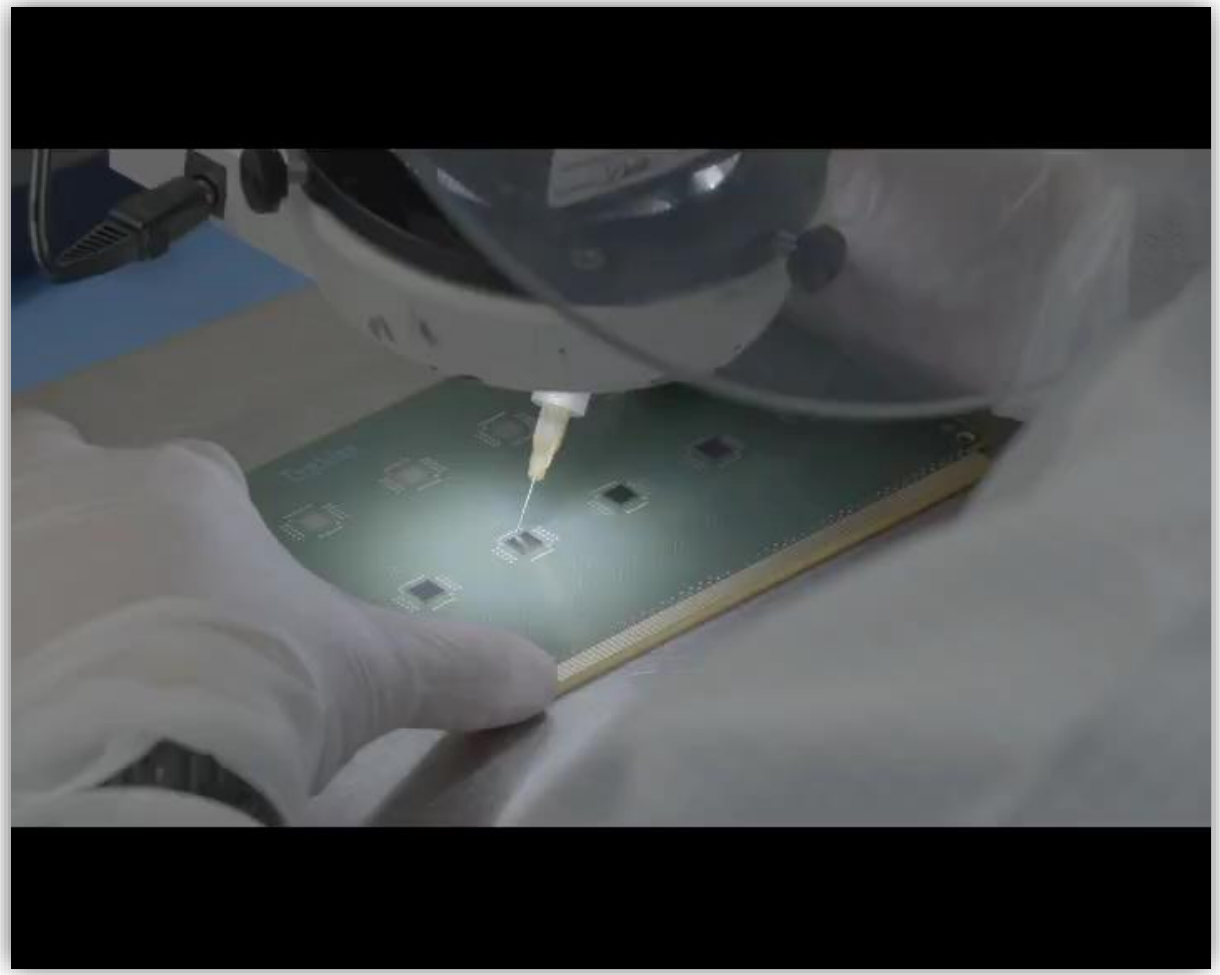
NOTE: There are variations as well.

Continuation of Flip Chip process

Plastic	Lidded
7. Mold	7a. Ball Attach
8. Mark	8a. Lid Mark
9. Singulate	9a. Lid Attach
10. Ball Attach	







Test and Qualification

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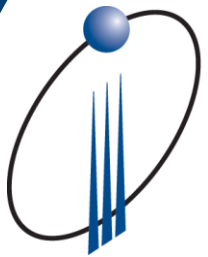

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Overall Recommended Electrical Test Methodology

Test the Device the Specified Performance Characteristics

- Functional at-speed
  - ✓ Application speed at a minimum may not need spec speed
  - ✓ Test frequency is a major tester cost driver
- Comprehensive functional testing
  - ✓ Test all device functionality
  - ✓ Fault grading is not possible
    - ➢ Only the manufacturer has device modeling capability
- Test key AC parameters
  - ✓ Key parameters are usually referenced to device clocks
    - ➢ Propagation delay
    - ➢ Setup and hold times
  - ✓ Use go-no-go testing to cover most AC parameters
    - ➢ Tested over the entire functional pattern
  - ✓ Selected AC characterization measurements can be made
- DC measurements to the full specified limits
  - ✓ Attempt to test 25C parameters at extended temperatures
  - ✓ Limit adjustments may be required after testing
- Select the appropriate tester
  - ✓ No one tester can effectively test all technologies

Flip Chip General Test Considerations

Test Considerations

- In wafer form, the bumps can be an issue at probe
  - ✓Make certain bumps are uniform across all pads
- Flip Chip parts are often faster and sometime hotter than standard IC technology – needing consideration of Junction temperature at test
  - ✓Thermal considerations at Package test and Burn-In / Life are key for many devices

Flip Chip General Qualification Considerations

- **Qualification Considerations**
  - Class Y Flip-Chip
    - Mil-PRF-38535 has inorganic substrate (ceramic), non-hermetic screening and qualification requirements for Space grade parts but can be tailored for military application
    - JC13.7 / SAE CE12 working on organic substrate non-hermetic screening and qualification requirements
  - Most Flip Chips are non-hermetics but it is typically not PEM also. Screening and Qual takes into consideration mechanical characteristic not typical of PEMs (Example: Constant Acceleration, Mechanical Shock etc.)
  - THB (85C/85% RH) vs. HAST – Mil PRF 38535 states to use 96 hrs. HAST (110C/85%RH). Many customers chose 1000 hours 85C/85% RH; a more benign but equivalent test
  - Flip Chip qualification also involves die pull and die shear test per Mil Std 883.
    - Die pull Flip chip pull off test TM 2031 or TM 2011. Our experience shows TM2011 condition is best suited for flip chip
    - Die shear Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 . Our experience shows TM2019 is best suited for flip chip
  - Consider performing construction analysis and pre-screen DPA to understand the manufacturing technology
  - Some concerns about vent holes (weeping holes) within Flip Chip during re-balling or moisture resistance tests. No issues found so far during qualification

Flip Chip General Qualification Considerations

Flip Chip Pull off Test

- **TM 2031:** The purpose of this test is to measure the strength of internal bonds between a semiconductor die and a substrate to which it is attached in a face-bond configuration
- **TM2011 Condition F:** 3.1.4 Test condition F - Bond shear (flip chip). This test is normally employed for internal bonds between a semiconductor die and a substrate to which it is attached in a face-bonded configuration. It may also be used to test the bonds between a substrate and an intermediate carrier or secondary substrate to which the die is mounted.

Die Shear Test

- **TM 2019:** The purpose of this test is to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to package headers or other substrates. This determination is based on a measure of force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization.
- **TM 2027:** The purpose of this test is to determine the strength of the element attachment system when subjected to force in the Y1 axis. This method is applicable to semiconductor die attached to headers or substrates by means of organic materials. Uses include material evaluations and process control.

General Qualification and Screening Considerations

Flip Chip Screening Considerations

TABLE I. . **100% Screening.** 1 2/

Test	MIL-STD-883 Test Method
Temperature cycling	1010, Cond B (-55°C to 125°C), 10 cycles minimum
Constant acceleration	2001, Cond E, Y1 orientation only
Serialization	
Electrical	Datasheet
Burn-in	1015, Cond D, 240 hours at T_j=125°C
Electrical	4.2.1 herein
Reverse bias burn-in	1015, Cond A or C, 144 hours at T_j=125°C
Electrical	Datasheet
Percentage defective allowable (PDA)	5% PDA, 3% functional at 25°C
Radiographic test	2012, one views
External visual inspection	2009
QCI/Qualification	Agreed upon plan

Note:

1/ Screening tests in accordance with MIL-PRF-38535 Class Y. The following tests are not required: Wafer lot acceptance test, nondestructive bond pull, internal visual, PIND, seal and radiation does rate induced latch-up test.

2/ Device junction shall not exceed 125°C.

Flip Chip Qualification Considerations

TABLE II. **QCI/Qualification.** 1/ 2/

Group	Test	MIL-STD-883 Test Method	Sample size
A	Electrical	Datasheet	116(0) or 100%
B-1	Physical dimensions	2016	3(0) can be rejects
B-2	Resistance to Solvent	2015	3(0)
	Flip chip pull off test	2031 or 2011	2(0)
	Flip chip die shear strength or substrate attach strength test	2019 or 2027	3(0)
B-3	Solderability	2003, max solder temp 220°C	22(0)from 3 devices
B-4	Ball shear	JESD22-B117	45(0)from 2 devices
C-1	Steady-state life test	1005, 1000 hours at T_j=125°C	5(0)
	Electrical	Datasheet	
D-3	Thermal shock	1011 Cond B, 15 cycles	5(0)
	Temperature cycling	1010 Cond C, 100 cycles	5(0)
	Moisture resistance	JESD22-A118 Cond B	5(0)
	Visual inspection	1004 or 1010	5(0)
	Electrical	Datasheet	5(0)
D-4	Mechanical shock	2002 Cond B	5(0)
	Vibration, variable frequency	2007 Cond A	5(0)
	Constant acceleration	2001 Cond E	5(0)
	Visual inspection	2009	5(0)
	Electrical	Datasheet	5(0)

Note:
1/ QCI/Qualification in accordance with MIL-STD-883 Test Method 5005 Class S. The following tests are not required: Internal water vapor content (B-1), internal visual and mechanical (B-2), bond strength (B-2), lead integrity (B-4), lead torque (B-4), salt atmosphere (D-5) and adhesion of lead finish (D-7).
2/ Device junction shall not exceed 125°C.

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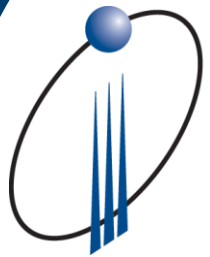

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