Advanced Packaging Overview – Design through Assembly and Test
FlipChip and Sip Packages

Presenters/Hosts (in order): Matt Bergeron, Richard McKee, Sultan Lilani, Jonathan Hochstetler

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October 2020

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Agenda/Topics Covered

1 Definition and Benefits of Flip Chip and SiPs

a) Flip Chip
b) SiP - System in a Package

2 Flip Chip

a) Bumping & RDL
b) Substrate
c) Implementations – packages variations
d) Assembly Considerations

3 SiP – System in a Package

a) Design considerations and trade-offs
b) What to include
c) Key Engineering considerations
d) Floor Plans
e) Substrates
f) Design Rules
g) Substrate
h) Assembly

4 Testing and Qualification

a) Test considerations
b) Complex Testing
c) Qualification Testing

Caveats & Acknowledgments

- **Caveats:**
  - Currently, there are lots of discussions about advanced packaging. This presentation is geared towards the most readily available technology (not necessarily the most exciting).

- **Acknowledgements:**
  - Integra Silicon Valley Package Engineering Staff
  - Integra Test Engineering
  - Doug Mathews – Advanced Microwave Products – ViaSat

Definition and Benefits of Flip Chip and SIPs

a) SIP

b) Flip Chip

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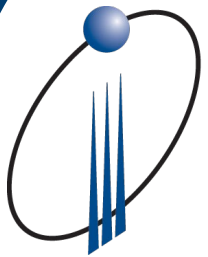

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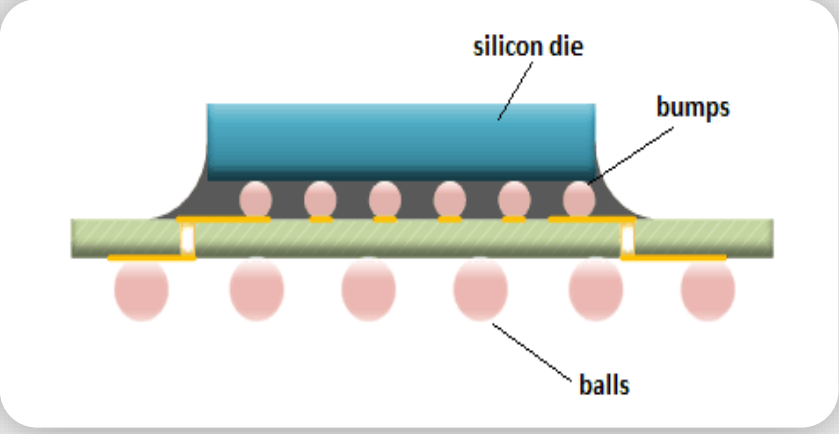
Flip Chip Definition

- Essentially, the name “Flip Chip” describes the method used to connect a semiconductor die to a substrate: The dies are bumped and then “flipped” onto a substrate, hence the name “Flip Chip”.



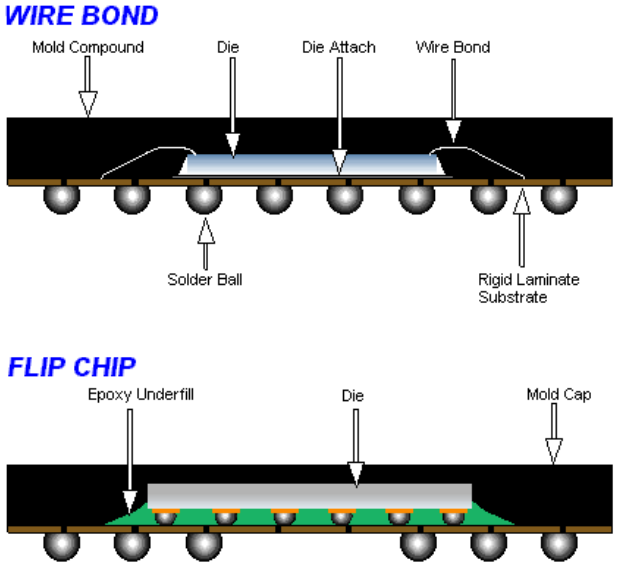
Fundamentals

- Bumps are placed directly on the die I/O pads typically distributed in an array across the entire die surface. This allows designers to place more pads per die, reduce the die size, and optimize signal integrity,
- Following the bumping process, the wafer may be thinned (back grinding), and then diced into individual die separated from the wafer.
- The bumped die is “flipped” onto the substrate. The bumps connect the die and the substrate together into a single package.

Flip Chip: Benefits

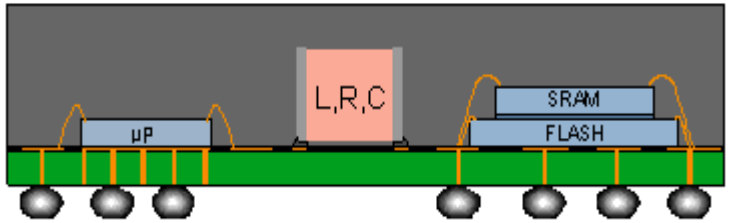
Flip Chip package technology offer a range of benefits including:

- High pin count
- High signal density
- Better power dissipation
- Low signal inductance, and good power/ground connectivity.
- Ideal for high speed interfaces (including RF) that wire bonds cannot support
- Good Assembly dynamics



SiP Definition

- The SiP performs all or most of the functions of an electronic system
- An example SiP can contain several chips—such as a specialized processor, DRAM, flash memory—combined with passive components—resistors and capacitors—all mounted on the same substrate.
- This means that a complete functional unit can be built in a multi-chip package, so that few external components need to be added to make it work



System-in-Package Benefits

- Simplifies the product system board
  - Layers and density
  - I/O count and pitch
- Increases functionality per unit area/volume
  - Reduced size
  - More performance in less space
- Improves Electrical Performance
  - Reduces parasitic
- Reduces Manufacturing Costs
  - Reduced component count
  - Inventory and carrying costs
  - Lower supplier support
  - Improve yield

- Improved Reliability
  - Solder joint reduction
- Lessens specialized expertise and testing requirements
  - Simplifies complex RF functions
  - Eliminates tuning at the system board level
  - Tested subsystem functions
- Improves time to market
  - Make changes to subsystem without (costly) changes to system board
  - Standardize subsystem “Macros” across a product family
- Can be a platform for derivative products

Note: Benefits can move to detriments if bad decisions are made on key considerations and trade-offs

Flip Chip

a) Bumping & RDL
b) Substrate
c) Implementations – packages variations
d) Assembly Considerations

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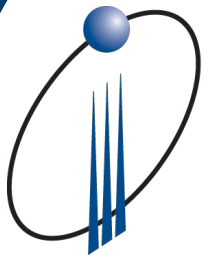

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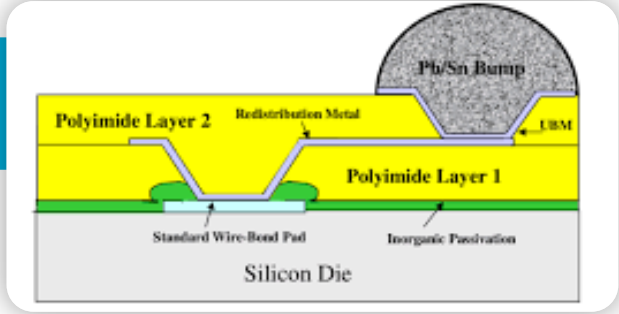
Flip Chip: Bump on Pad & RDL

Wafer Bumping can be considered as a step in wafer processing where solder spheres are attached to the I/O pads.



Wafer Bumping Technology

- Some wafers are designed to be flip chips and bumps go directly on pads.
- A Redistribution layer (RDL) is added to a wirebond die to establish bumps that are compatible with the assembly of a die on a Printed Circuit board
- Paste-printed bumps, plated bumps, or placed preformed solder spheres are typically mounted onto a fluxed, under bump metallization (UBM) material, that is plated or sputtered onto the die pads (Al or Cu), to insure good adhesion of the bumps.
- Wafer bump compositions: gold, eutectic, lead tin, lead free, high lead materials, or Cu pillar. The bump size and bump pitch may vary depending on pad count, signal integrity, and assembly design rules.

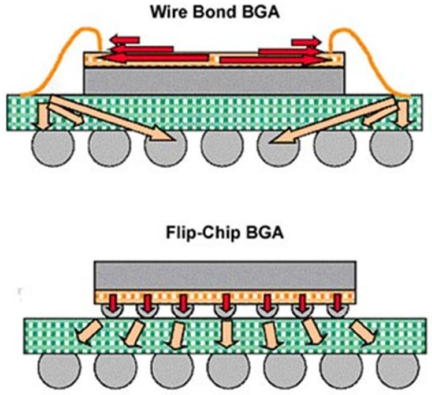
Flip Chip: Substrate Overview

Substrate Technology

- Substrates can be made by different PCB materials: laminate, build-up, organic, ceramic, and more. Substrate layout design rules vary from different suppliers.
- The substrate provides the connectivity to the external PCB via solder balls (typically larger than the bumps, on a broader pad pitch).
- The substrate size, number of layers and material properties have direct impact on the total package cost. In some cases the substrate can be the most expensive element in a Flip Chip package.
- Substrate design consists of layout of all signals from the package external balls to the bumped internal pads.
- Substrates can consist of many layers ranging from 2-18 layers to allow proper routing of all signals for enhanced device performance

Flip Chip Size Considerations

- Is there enough room to actually route the connections from the bumps to the solder balls that connect to the PCB?
- The smaller the substrate vs. the die, the higher the cost in many cases



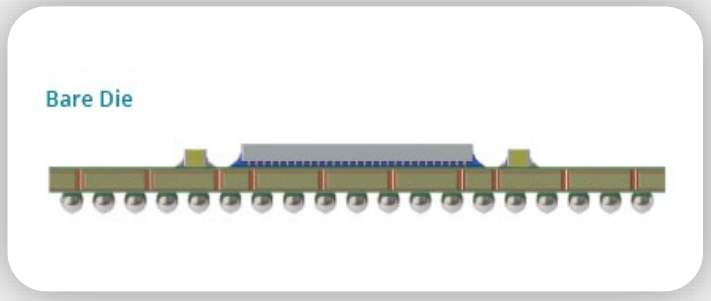
Flip Chip: FCBGA - Package Example

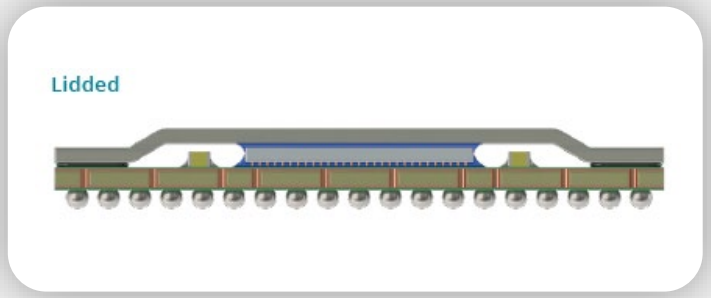
FCBGA – Flip Chip Ball Grid Array

- Flip Chip BGA packages: Still the most common package for bumped dies.

- Advantages:
- Good thermal performance, and scalability for large and complex dies.
- Low cost FCBGAs use a laminate (PCB type) substrate.
- Build-up substrates are also an option, offering –
- Finer pitch routing, enhanced signal and thermal performance, and a lower profile, at a cost.

- FCBGA is the preferred flip chip solution for high power designs and designs with a large number of balls (over 100, for example).



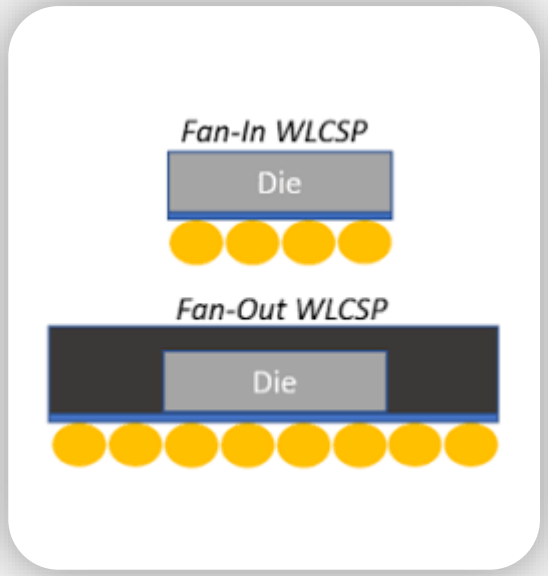


Flip Chip: WLCSP - Package Example

WLCSP – Wafer Level Chip Scale Package – NO Substrate

- **FAN-IN**
  - Wafer Level Chip Scale Package (WLCSP) is a die-sized package with bumps that are essentially balls that can be soldered directly to a PCB.
  - Bump on Pad (BOP): Solder bumps attached directly to the die pad openings, that gives the shortest path from die circuit to PCB, so achieves optimum signal performance, lowest inductance, highest speed).
  - Preferred solution for low-power, low ball count devices where the small form factor is an advantage.

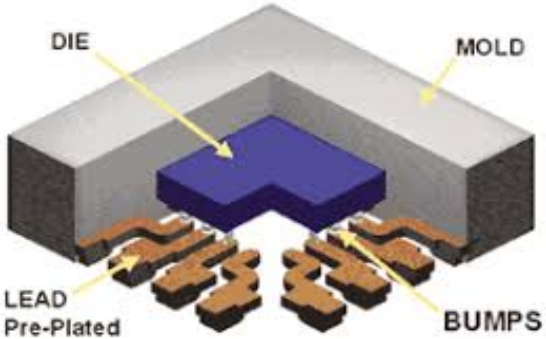
- **FAN-OUT**
  - eWLB is similar to the WLCSP, however the wafers are first diced, the dies spaced apart on tape & frame, and a resin material is flowed over the dies then hardened to form a re-constituted wafer.
  - Referred to as “Fan Out” because the relatively small pitch die pads are able to be routed out (fanned out) to a larger pitch array of balls over the peripheral epoxy resin.



Flip Chip: QFN - Package Example

FCQFN – Flip Chip Quad Flat No Lead

- Flip Chip QFN packages: Copper Leadframe with overmold replaces use of laminate substrate in this popular package for bumped dies. Advantages -
- Self-inductance & capacitance: 60% improvement.
- 15% lower thermal resistance.
- 30x reduction in resistance vs wire bond.
- Withstands 260°C solder shock test.
- Finer pitch routing, enhanced signal and
- thermal performance, with a lower profile.
- FCQFN is the preferred flip chip solution for:
- Wireless Devices.
- Power Management Devices.
- High-speed Network Devices.



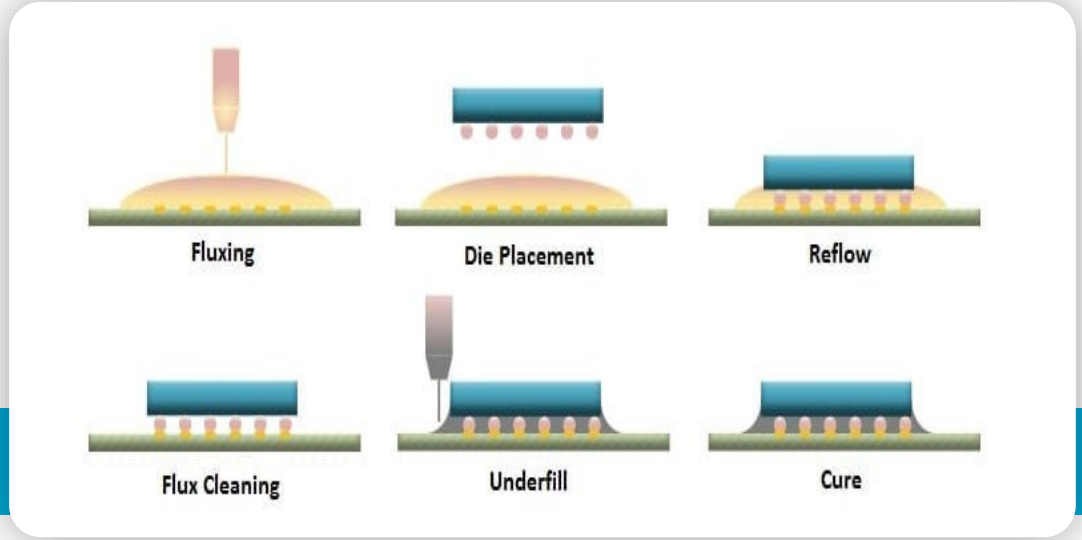
Flip Chip: Assembly Process (FCBGA)

Flip Chip Assembly Process

In order for the chip to be connected or mounted to a substrate, the die is turned or flipped over and brought into alignment with the pads located on the substrate.

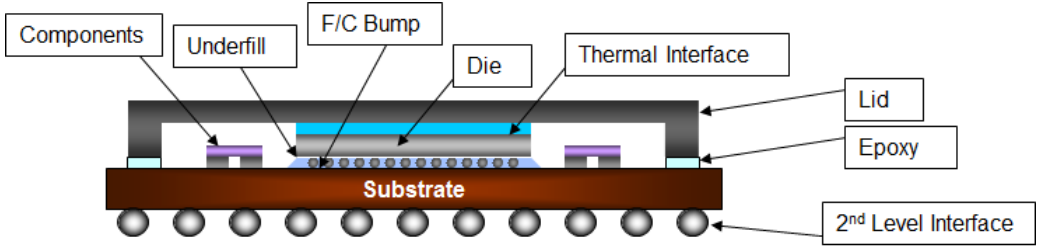
There are six (6) key process steps:

1. **Fluxing**
2. **Placement**
3. **Reflow**
4. **Flux Cleaning**
5. **Capillary Underfill**
6. **Cure**



NOTE: There are variations as well.

Flip Chip: Assembly Considerations

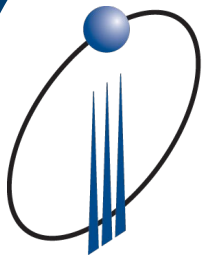


Description	Options	Details / Experience
Substrate	Ceramic, Organic laminate, Flex Circuit, PCB	
Die	Si / SiGe / GaAs / Low K	I/O = 3 min to ~ X (bumps)
Lid / Heat Spreader	Ceramic /Aluminum / Cu	
	Lid Stiffner / No lid	
Thermal Interface	Grease / Gel / Adhesive	
Underfill	Namics 8439-1 / Other(s)	
SMT Components	Resistors, Capacitors, etc. *(high quantities are subject to review)*	Conductive epoxy / Solder
F/C Bump	Eutectic PbSn: 37/63	Pitch = 125um min
	SAC or other Pb-free	Pitch = 125um min
	High Pb: 90/10, 95/5, 97/3	Pitch = 125um min
2nd Level Interface	LGA	Pitch = 0.4 mm min
	BGA [Eutectic / Pb-free]	Pitch = 0.4 mm min
Substrate Metalization	Ceramic	Ni/Au
	Organic	Solder on Pad (SOP) / ENiG

SiP – System in a Package

a) Design considerations and trade-offs
b) What to include
c) Key Engineering considerations
d) Floor Plans
e) Substrates
f) Design Rules
g) Substrate
h) Assembly

3



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K.I.S.S. Rule

- **The more complex you make a system/package = the more challenges to overcome**
- **Some of the Challenges:**

Challenge #1 – Can I actually make the substrate work? (thickness, performance, widths and space/cost)

Challenge #2 – Can I procure the parts needed in the formfactor that will work (can you get die?)

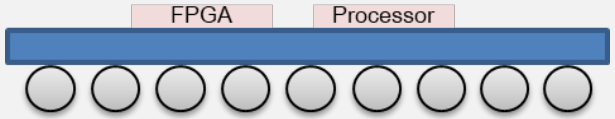
Challenge #3 – Mathematically the more components you have in a system the more likely a failure. Simple example: 1 die in a flip chip & 90% typical yield = 90% Yield
5 die in a SiP and 90% yield on each = 59% yield
(.9x.9x.9x.9x.9)

Challenge #4 - Reliability. The mix and match of components, shields, die, etc. can create stresses at the package or board level.

Challenge #5 - Testability -Testability has to be designed in from the beginning.

Use & Needs & Parameters

Initial questions that need to be asked



- What is the package envelope (space x, y & z)
- What is the goal of the SiP
  - Is it to reduce cost, size, increase performance, eliminate a vendor, improve reliability?
- What is the application & outside parameters of all considerations?
  - SiP by itself won't save cost, but in combination with system partitioning, can significantly reduce the total BOM count at the product/board level.

The answers will give you a target design and assist on trade-offs

- **Key:** Understanding this will give the design team a better target for trade-offs that may come during the design phase

Key Considerations : Making the Right Engineering Tradeoffs

System Partitioning- Determines flexibility of the package and ability to optimize the package.

- 80% of the cost is defined in the first 20% of the design cycle.
- Firm Chip I/O locations limits flexibility, but faster schedule
- Flexible Chip I/O locations adds development time (IC's in design)
- Die and Package Co-Design optimum for Cost Size and Performance, Build to print optimum for time.

Package Requirements/Constraints

- Max height, Size, Thickness
- Die Count and size
- System Passives and counts on SiP/MCM
- Packaged parts on SiP or MCM (Clocks, buffers, regulators)
- MSL Level
- **Thermal Constraints → Thermal enhancements**
- Warpage
- Environmental & Qualification
- Solder Hierarchy- internal & external joints

Key Considerations : Making the Right Engineering Tradeoffs

Critical I/Os

- Analog, RF, SERDES, DA/AD, Differential, single ended, Impedance levels, High speed memory I/Os , Reference Clocks, PCIe, JTAG etc.

- Die Considerations- Die Count and Area will drive overall SiP/MCM size.

- Technology (CMOS, GaN, GaAs, BiCMOS) - Low K, geometry, thickness
- Die Attach
- Interconnect Technologies - Wirebond type and diameter
  - ✓ Gold, Copper, Aluminum (power products)
  - ✓ Wirebond assembly rules
  - ✓ Surface metallization
  - Flip Chip
  - Ball Pitch, Count, Diameter, Composition, underfill keepout
- Thickness of die, Flip Chip or Wirebond rules, Substrate line and spacing.
- I/O Configuration and location (determines inter-routability)
- Power Dissipation

Key Considerations : Making the Right Engineering Tradeoffs

Substrates

- Semiconductor Laminates
  - ✓ Laminate Type BT, ABF, RFBTs
  - ✓ Dk & Df
  - ✓ Subtractive, Semi-Additive, Buildup
  - ✓ L/S, Via size, capture pad, filled vias, bump on via.
  - ✓ Top Side Metallization Copper OSP, wirebondable gold, CuOSP over SOP, Gold over Copper
- Ceramics- HTCC or LTCC
- Glass

Assembly

- Array, single unit assembly (larger SiPs)
- Underfill keep-outs
- Wirebond keep-outs
- Component spacing
- Overmolded Considerations
- Shielding types and rules
- Front side, back side components
- SiP and Application board routing/escapes.

Key Considerations : Making the Right Engineering Tradeoffs

Encapsulation – Overmolded , Underfill, Dam and Fill, metal lid

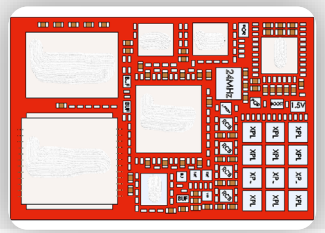
Test - KGD- Die must be Known Good or Known Tested Die

- ✓ Cumulative yields for each die, plus package assembly and test yield
- ✓ Plan for wafer level testing

- Package DFT, BIST, JTAG
  - ✓ Additional Test I/Os at the package level
- Sockets and Performance impact at test.
  - ✓ High Speed Sockets
  - ✓ Thermal Management
  - ✓ RF Test Ports
- Programming memory
  - ✓ Pre and Post assembly

Floor Plans – Important consideration for SiP

- **Die I/O Configuration, Signal Integrity, thermal planning and other considerations drive Floor Plans**
- Some trade-offs and considerations:
  - ***Separation of thermally sensitive die such as DDR and FLASH from Power Supply components***
    - Memory limits maximum junction temperature to 85˚C
    - Processor and logic can run up to ~100˚C
    - Power supply parts may run up to 125˚C
  - Rectangular substrate vs. Square
  - Passives in SiP
    - Need inside vs. on board
    - Size of Passives



- **Other discussions and solutions:**
  - Move as many inductors off-package as possible
    - For RF this may be more of move as many on as possible.
  - Package-on-Package (POP) for DDR
  - Increases overall package thickness
  - Mount some passives on bottom of substrate
    - Requires ball depopulation
  - Reduce DDR and NAND chip sizes if possible
  - Wirebonds require spacing for manufacturability
  - Use an external DDR/FLASH combo package, mounted on the backside of the motherboard
    - Drives I/O count and routing out of the package- trade
  - Stack capacitors of same form-factor
  - Stacking of Die – FC and Wirebond mix
  - Flip Chip die require underfill and room to underfill

Substrates & Design Rules

SUBSTRATE DESIGN RULES

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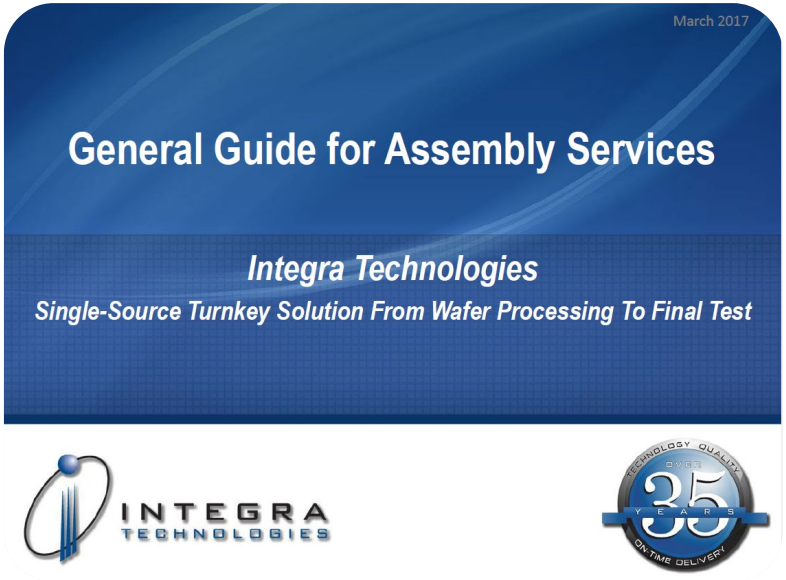


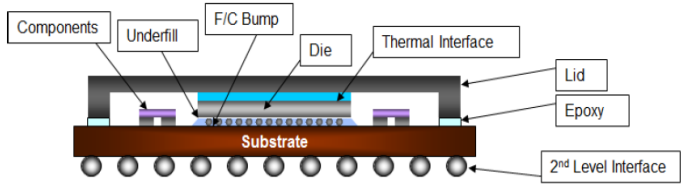
Design Rules

- Interaction between Assembly rules and Substrate rules
- Just because it works for one – doesn't mean it works for both
- Example – surface finish

FLIP CHIP FEATURES *Confidential*

SURFACE FINISH	Electroless Nickel Gold, Au : min 0.3 µm
	ENIG (Electroless Nickel Immersion Gold), Au : min 0.03 µm
	OSP (Organic Surface Preparation) : Glicoat - SMD F2(LX)
	SOP (Solder On Pad)
BUMP PAD TOP CO-PLANARITY	maximum 30 µm / Unit

Table 18. Flip Chip Surface Finish



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	BGA [Eutectic / Pb-free]	Pitch = 0.4 mm min
Substrate Metalization	Ceramic	Ni/Au
	Organic	Solder on Pad (SOP) / ENiG

RoHS Compliant

Cost Drivers of Substrates

Cost Drivers & Elimination of Vendors

- More layers
- Larger area
- Exotic connections between layers
- Higher aspect ratios
  - ✓ Small holes through thick substrate
- Special tolerances
- Smaller features
  - Lines and spaces

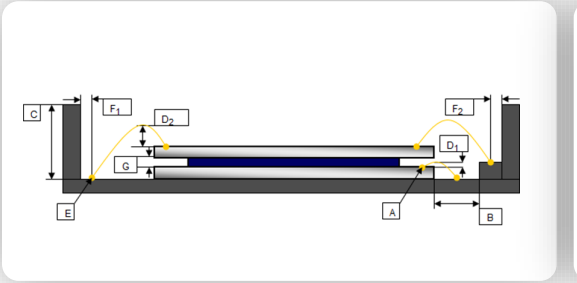
(Unit : μm unless noted)

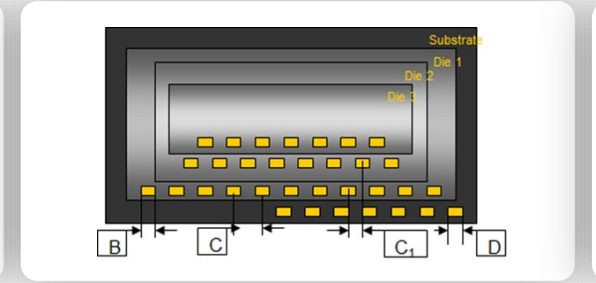
ITEM			SPECIFICATIONS & TOLERANCE	
			Standard	Special
Core Material		Type	HL832, HL832HS, E679BR, E679F, E679FB	HL832NX *, E679FGB *
		Thickness	100, 150, 200	60, 80, 400
Cu Foil Thickness		Outer	9, 12, 18 (1/4 oz, 3/8 oz, 1/2 oz)	36 **, 70 *** (1 oz, 2 oz)
		Inner	12, 18, 36 ** (3/8 oz, 1/2 oz, 1 oz)	70 *** (2 oz)
Prepreg (with woven glass)		Type	GHPL830, GHPL830HS, GEA679W, GEA679F	GHPL830NX *,GEA679FG *
		Thickness	60, 100	40, 45, 50
RCF (RCC)		Thickness	50, 60, 65, 80	70, 85
Drill/Pad Size	Through Hole (Mechanical)	Outer	120/270, 150/300, 200/375, 250/450	120/250 (Core ≤ 150), 100/230 (2 L)
		Inner	150/450, 200/500	120/370, 150/400, 200/450
		Aspect Ratio	3.0	- - -
	CO_2 Laser	Outer	100/250, 130/300 (Bottom Cu ≥ 18)	80/200
		Inner	100/250	80/200
		Aspect Ratio	0.7	- - -
Layer to Layer Metal Alignment			+/- 75	+/- 50
Line/Space		Outer	50/50	35/35
		Inner	75/75	50/50
Copper Plating (Through Hole Wall) Thickness (Electroless Cu)			10 +/- 5, 15 +/- 5, 20 +/-5	25 +/- 5, 30 +/- 5, 35 +/- 5
Plugging Ink		Type	HBI200, AE1125 *, THP100DX1 *	AE3030
Solder Resist		Type	AUS5, AUS7, AUS308 *,AUS310 *	AUS402 *, SR7200G *, S-500
		Thickness	15 +/- 10, 20 +/- 10, 25 +/- 10	30 +/- 10, 35 +/- 10 (Double Coating)
		Opening Size	150 (minimum)	90 **** (minimum)
		Min. Width	100 (minimum)	80 (minimum)
		Registration	+/- 50	+/- 37.5
Surface Finish		Type	Soft Bondable Au, Hard Au *****	OSP, SOP, Direct Au (without Ni) ******
		Plating	Electrolytic, Electroless	- - -
Plating Thickness		Nickel	3, 5 (minimum)	- - -
		Gold	0.3, 0.5 (minimum), 0.03 (ENIG)	- - -
Capped Via Finished		Line Width	60 +/- 25	50 +/- 25
		Cu Thickness	25 +/- 8	21 +/- 8
Board Twist / Bow			1.0 % per strip (maximum)	0.5 % per strip (maximum)
Board Parallelity			+/- 100	- - -
Tooling Hole to Tooling Hole (min: 1mm)			+/- 50 (0 ~ 200 mm)	- - -
Tooling Hole to Strip Edge			+/- 50 (0 ~ 50 mm)	- - -

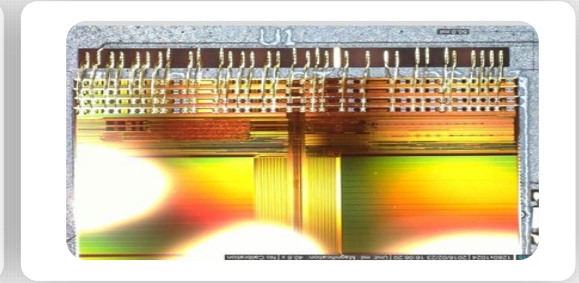
* Halogen Free Type
** Line / Space ≥ 100 / 100 mm
*** Line / Space ≥ 150 / 150 μm
**** Solder Resist Thickness : 10 μm
***** Electrolytic Plating only
****** Electroless Immersion Plating only

Stacking Die – Space saving

- Die Stacking is the process of mounting multiple chips on top of each other within a single semiconductor package.
  - Die stacking, which is also known as 'chip stacking', significantly increases the amount of silicon chip area that can be housed within a single package of a given footprint.
  - Aside from space savings, die stacking also results in better electrical performance of the device, since the shorter routing of interconnections between circuits results in faster signal propagation and reduction in noise and cross-talk.
- There are a number of approaches – some blended with flip chip



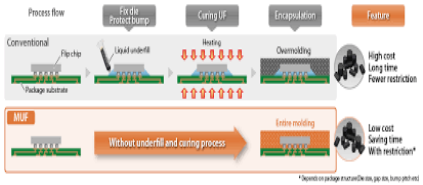




Note: There are other considerations such a true 3D stacking that are not discussed here

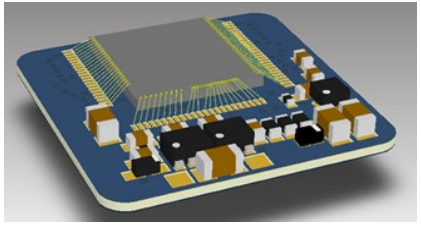
Encapsulation considerations

- **Open Cavity**
  - Great RF insulation (especially when coupled with ground plane)
  - Sometimes easier to make
  - In volume likely more expensive
- **Plastic encapsulation/Glob Top / Dam & Fill**
  - Can be least expensive
  - Can interact poorly with SiP components such as plastic parts
- **Flip Chip**
  - Underfill/No Underfill?
  - Bump considerations in Mil/Aero applications (tin wiskers)



Glob Top Encapsulation Process and Result:

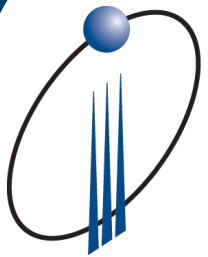
Dam & Fill (Frame & Fill) Encapsulation Process and Result:



Testing and Qualification

a) How do I test and qualify this Package

4



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General Testing Considerations

SiP Test Considerations

- Evaluate the SiP Design and consider if it should be classified as
  - ✓ Application Specific IC
  - ✓ Hybrid IC
- SiP by definition will have complex functional test requirements
- Plan on spending a considerable amount of time on the testing plan
  - ✓ Testing the appropriate parts of each portion of the SiP
- Characterization and Production plans may vary radically (as with normal products)

Flip Chip Test Considerations

- In wafer form, the bumps are often an issue at probe
  - ✓ Advance consideration is required
- Flip Chip parts are often faster and sometime hotter than standard IC technology – needing consideration of Junction temperature at test
  - ✓ Thermal considerations at Package test and BI are key for many devices

SiP Electrical Testing

Keys to cost-effective electrical test solutions:

- Early engagement with SIP designers to ensure design incorporates features for appropriate test coverage. These include access points, test modes etc.
- Leverage SCAN Chain and JTAG solutions using digital vectors from simulations.
- Focus on verifying connectivity of SIP components and interactions between SIP components, not necessarily performance of each parameter of individual SIP components
- Consider temperature performance of entire SiP due to the limitation of temperature performance of each component of the SiP
  - ✓ One component of the SiP may limit the operating temperature of entire SiP
- Test to usage conditions like speed and temperature extremes.

Flip Chip FPGA Test Methodology

Integra Implements Designs into the FPGA to Support Functional and Parametric Testing

- Test develops independent of manufacturer proprietary test methods
- Integra uses in-house tools from the manufacturer
- Create the test vectors and configuration vectors for the 93K tester
- Functional at-speed testing (using design modeling not datasheet)
  - ✓ Datasheet AC specs are internal FPGA performance characteristics
  - ✓ AC parameter tests will be generated from Xilinx software simulations
- Designs implementation includes comprehensive DC parameters
- Develop functional vectors verifies design and device functionality

Overall Recommended Electrical Test Methodology

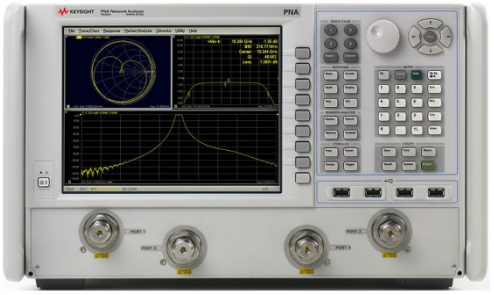
Test the Device the Specified Performance Characteristics

- Functional at-speed
  - ✓ Application speed at a minimum may not need spec speed
  - ✓ Test frequency is a major tester cost driver
- Comprehensive functional testing
  - ✓ Test all device functionality
  - ✓ Fault grading is not possible
    - ➢ Only the manufacturer has device modeling capability
- Test key AC parameters
  - ✓ Key parameters are usually referenced to device clocks
    - ➢ Propagation delay
    - ➢ Setup and hold times
  - ✓ Use go-no-go testing to cover most AC parameters
    - ➢ Tested over the entire functional pattern
  - ✓ Selected AC characterization measurements can be made
- DC measurements to the full specified limits
  - ✓ Attempt to test 25C parameters at extended temperatures
  - ✓ Limit adjustments may be required after testing
- Select the appropriate tester
  - ✓ No one tester can effectively test all technologies

Electrical Testing equipment

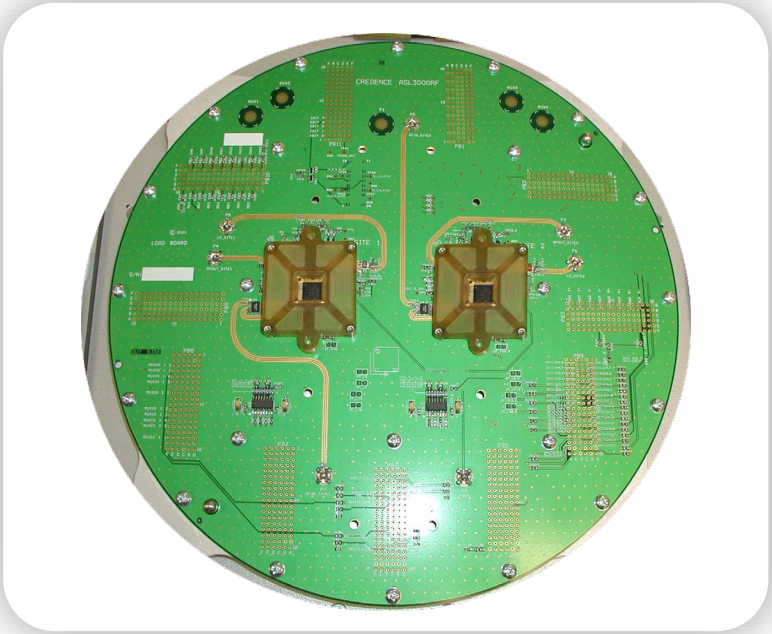
Integrate industry standard Automated Test Equipment (ATE) with auxiliary equipment to augment capabilities.

Examples: Credence ASL3000 + 50GHz RF Network Analyzer



Electrical Testing equipment

- Implement parallel test solutions and automated handling of product during testing when possible to keep cost of test low.



SiP Qualification Considerations

- Evaluate the SiP Design and consider if it should be considered
  - Application Specific IC
  - Hybrid IC
  - Look for Mil-PRF-38534 and Mil-PRF-38535 for screening and qualification guidance
- Most SiPs use non-packaged die
- Consider material characteristic of the SiP product (example: organic substrate vs. ceramic substrate) – CT and Environment consideration
- Consider performing contraction analysis and pre-screen DPA to understand the manufacturing technology

Flip Chip Qualification Considerations

- Most Flip Chips are non-hermetics
- Class Y Flip-Chip
  - Mil-PRF-38535 has inorganic substrate (ceramic), non-hermetic screening and qualification requirements for Space grade parts but can be tailored for military application
  - JC13.7 / SAE CE12 working on organic substrate non-hermetic screening and qualification requirements
- Consider performing contraction analysis and pre-screen DPA to understand the manufacturing technology

Typical Screening Plan – Flip Chip

TABLE I. . **100% Screening.** *1* 2/

Test	**MIL-STD-883 Test Method**
Temperature cycling	1010, Cond B (-55°C to 125°C), 10 cycles minimum
Constant acceleration	2001, Cond E, Y1 orientation only
Serialization	
Electrical	Datasheet
Burn-in	1015, Cond D, 240 hours at T_j=125°C
Electrical	4.2.1 herein
Reverse bias burn-in	1015, Cond A or C, 144 hours at T_j=125°C
Electrical	Datasheet
Percentage defective allowable (PDA)	5% PDA, 3% functional at 25°C
Radiographic test	2012, one views
External visual inspection	2009
QCI/Qualification	Agreed upon plan

Note:

1/ Screening tests in accordance with MIL-PRF-38535 Class Y. The following tests are not required: Wafer lot acceptance test, nondestructive bond pull, internal visual, PIND, seal and radiation does rate induced latch-up test.

2/ Device junction shall not exceed 125°C.

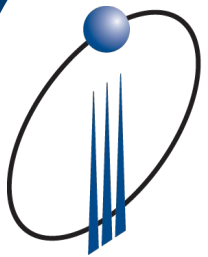
Typical Qualification Plan – Flip Chip

TABLE II. **QCI/Qualification.** 1/ 2/

Group	Test	MIL-STD-883 Test Method	Sample size
A	Electrical	Datasheet	116(0) or 100%
B-1	Physical dimensions	2016	3(0) can be rejects
B-2	Resistance to Solvent	2015	3(0)
	Flip chip pull off test	2031 or 2011	2(0)
	Flip chip die shear strength or substrate attach strength test	2019 or 2027	3(0)
B-3	Solderability	2003, max solder temp 220°C	22(0)from 3 devices
B-4	Ball shear	JESD22-B117	45(0)from 2 devices
C-1	Steady-state life test	1005, 1000 hours at T_j=125°C	5(0)
	Electrical	Datasheet	
D-3	Thermal shock	1011 Cond B, 15 cycles	5(0)
	Temperature cycling	1010 Cond C, 100 cycles	5(0)
	Moisture resistance	JESD22-A118 Cond B	5(0)
	Visual inspection	1004 or 1010	5(0)
	Electrical	Datasheet	5(0)
D-4	Mechanical shock	2002 Cond B	5(0)
	Vibration, variable frequency	2007 Cond A	5(0)
	Constant acceleration	2001 Cond E	5(0)
	Visual inspection	2009	5(0)
	Electrical	Datasheet	5(0)

Note:
1/ QCI/Qualification in accordance with MIL-STD-883 Test Method 5005 Class S. The following tests are not required: Internal water vapor content (B-1), internal visual and mechanical (B-2), bond strength (B-2), lead integrity (B-4), lead torque (B-4), salt atmosphere (D-5) and adhesion of lead finish (D-7).
2/ Device junction shall not exceed 125°C.

THANK YOU



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Sales Contact information:

www.integra-tech.com

sales_inquiry@integra-tech.com

https://www.linkedin.com/company/integra-technologies-llc/

https://www.integra-tech.com/contact